instruction supplying means for supplying, in succession from said instruction register, said one or more sequential instructions of said first of said instruction groups to said central processing unit;

instruction decoding means for configuring said instruction supplying means to select from said instruction register an operand associated with one of said instructions from said first of said instruction groups.

72(Twice Amended). The microprocessor system of claim 71 wherein said instruction decoding means further includes means, responsive to a SKIP instruction in said instruction register, for configuring said instruction [supplying means to skip one or more of said one or more sequential instructions during transfer thereof] fetching means such that the next instruction group is supplied to the instruction register, and for configuring said instruction supplying means to supply in succession from said instruction register, said one or more sequential instructions, beginning with the first instruction in said instruction register from said next instruction group, to said central processing unit.

73(Twice Amended). The microprocessor system of claim 72 further comprising:

means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction [supplying] decoding means to said SKIP instruction based on existence of said predefined condition.

74(Twice Amended). The microprocessor system of claim 71 further comprising:

a loop counter that is connected to receive a decrement control signal from said instruction decoding means, said instruction decoding means further including means, responsive to a MICROLOOP instruction in said instruction register, [being] configured to supply said decrement control signal to said loop counter [in response to a MICROLOOP instruction within one of said one or more sequential instructions received from said instruction supplying means], said instruction supplying means being configured to supply from said instruction register said one or more sequential

instructions, beginning with the first instruction in said instruction register, from said first of said instruction groups, to said central processing unit.

77(Twice Amended). The microprocessor system of claim 71 wherein said instruction decoding means includes means for supplying control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied to said instruction register, and for configuring said instruction supplying means to supply to said central processing unit a remainder of [a current one] said first of said instruction groups as [another] said operand.

78(Twice Amended). The microprocessor system of claim 71 wherein said instruction decoding means configures said instruction supplying means to supply to said central processing unit a last byte of [a current] said first of said instruction groups as [another] said operand in response to one of said one or more sequential instructions within said [current one] first of said instruction groups.

91(Amended). A microprocessor [system] comprising:

a central processing unit;

an instruction register operatively coupled to said central processing unit;

instruction fetching means for providing instruction groups to said instruction register wherein certain of said instruction groups include one or more operands or sequential instructions or both; said one or more sequential instructions including at least one instruction that accesses operands or instructions or both , said operands and instructions being located relative to said instruction groups;

instruction supplying means for successively coupling said one or more sequential instructions of said certain of said instruction groups to said central processing unit; and

instruction decoding means for configuring said instruction supplying means to select operands from said instruction register associated with particular ones of said sequential instructions.

92(Amended). The microprocessor [system] of claim 91 wherein said instruction decoding means, upon receiving a SKIP one of said one or more

sequential instructions from a current one of said instruction groups, configures said instruction fetching means to fetch a next one of said instruction groups to said instruction register [from a memory of said microprocessor system], and configures said instruction supplying means to supply a first of one of said one or more sequential instructions.

93(Amended). The microprocessor [system] of claim 92 further including means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction [supplying] decoding means to said SKIP instruction based on existence of said predefined condition.

94(Amended). The microprocessor of claim 91 [wherein said instruction supplying means includes] further comprising a loop counter, said instruction decoding means, responsive to a MICROLOOP instruction within said instruction register, providing a decrement signal to said loop counter [in response to a MICROLOOP instruction within said instruction register], and said instruction supplying means being configured to supply from said instruction register said one or more sequential instructions, beginning with the first instruction in said instruction register, from a current one of said instruction groups, to said central processing unit.

95(Amended). The microprocessor [system] of claim 94 further comprising:

means for determining whether a predefined condition exists within said microprocessor system, and

means for controlling response of said instruction decoding means to said MICROLOOP instruction based on existence of said predefined condition.

96(Amended). The microprocessor [system] of claim 91 wherein said instruction decoding means includes means, responsive to ones of said sequential instructions of predetermined type, for supplying control signals to said instruction

fetching means such that a subsequent one of said instruction groups is provided to said instruction register.

97(Amended). In a microprocessor system including a central processing unit, memory, and an instruction register, a method for providing instructions from said instruction register to said central processing unit comprising the steps of:

providing instruction groups to said instruction register from said memory wherein certain of said instruction groups include one or more operands or sequential instructions or both, said operands and instructions being located relative to said instruction groups;

supplying, in succession from said instruction register, said one or more sequential instructions of said certain of said instruction groups to said central processing unit; and

selecting[, in accordance with position in said instruction register of one of said instructions of one of said instruction groups,] an operand from said one of said instruction groups for use by said central processing unit.

99(Amended). The microprocessor [system] of claim 91 wherein said instruction decoding means are configured to supply control signals to said instruction fetching means such that a subsequent one of said instruction groups is supplied as an operand in response to one of said one or more sequential instructions.

100(Amended). The microprocessor [system] of claim 96 further comprising means for determining whether a predefined condition exists within said microprocessor system, and means for controlling response of said instruction decoding means to branch-type ones of said instructions based on existence of said predefined condition.

Cancel claim 76.